

IN THE SPECIFICATION:

Please insert the following section at page 1, line 5 of the Specification:

**CROSS-RELATED APPLICATIONS**

*CJ* This application is a Divisional application of U.S. Patent Application Serial No. 09/173,288, filed October 14, 1998.

IN THE DRAWINGS:

Please delete sheets "5/13", "6/13", and "7/13" and replace with the figures attached hereto.

IN THE CLAIMS:

Please cancel claims 1-12.

Please replace claims 15-21 with the following amended claims:

*AP* 1 15. (As Amended) The multilayer ceramic substrate of claim 13, wherein a  
2 meshed pattern is provided in a part of said conductive pattern.

*AP* 1 16. (As Amended) The multilayer ceramic substrate of claim 13, wherein a  
2 shield pattern is provided at an outer edge of said conductive pattern.

*AP* 1 17. (As Amended) The multilayer ceramic substrate of claim 13, wherein  
2 said ceramic substrate is provided with a through hole filled with an  
3 electroconductive substance and burned, and said via is disposed on the through  
4 hole.

*AP* 1 18. (As Amended) The multilayer ceramic substrate of claim 13, further  
2 comprising a dielectric layer formed on a part of said ceramic substrate.

*AP* 1 19. (As Amended) The multilayer ceramic substrate of claim 13, further  
2 comprising an LSI chip mounted on a part of one of said first and second  
3 conductive patterns with the face down and electrically connected.

1        20. (As Amended) The multilayer ceramic substrate of claim 13, further  
2 comprising an LSI chip mounted on a part of one of said first and second  
3 conductive patterns with the face down and electrically connected through an  
4 electroconductive paste applied on the top of a fine bump provided on one of said  
5 first and second conductive patterns, said fine bump formed by using a second  
6 groove which is disposed on said intaglio at a place corresponding to a pad of said  
7 LSI chip

1        21. (As Amended) The multilayer ceramic substrate of claim 13, further  
2 comprising an LSI package mounted on a part of one of said first and second  
3 conductive patterns with the face down and electrically connected through a lattice  
4 of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said  
5 first and second conductive patterns.

1        Please add the following new claims:

1        22. (Newly Added) The multilayer ceramic substrate of claim 14, wherein  
2 a meshed pattern is provided in a part of said conductive pattern.

1        23. (Newly Added) The multilayer ceramic substrate of claim 14, wherein  
2 a shield pattern is provided at an outer edge of said conductive pattern.

1        24. (Newly Added) The multilayer ceramic substrate of claim 14, wherein  
2 said ceramic substrate is provided with a through hole filled with an  
3 electroconductive substance and burned, and said via is disposed on the through  
hole.

1        25. (Newly Added) The multilayer ceramic substrate of claim 14, further  
2 comprising a dielectric layer formed on a part of said ceramic substrate.

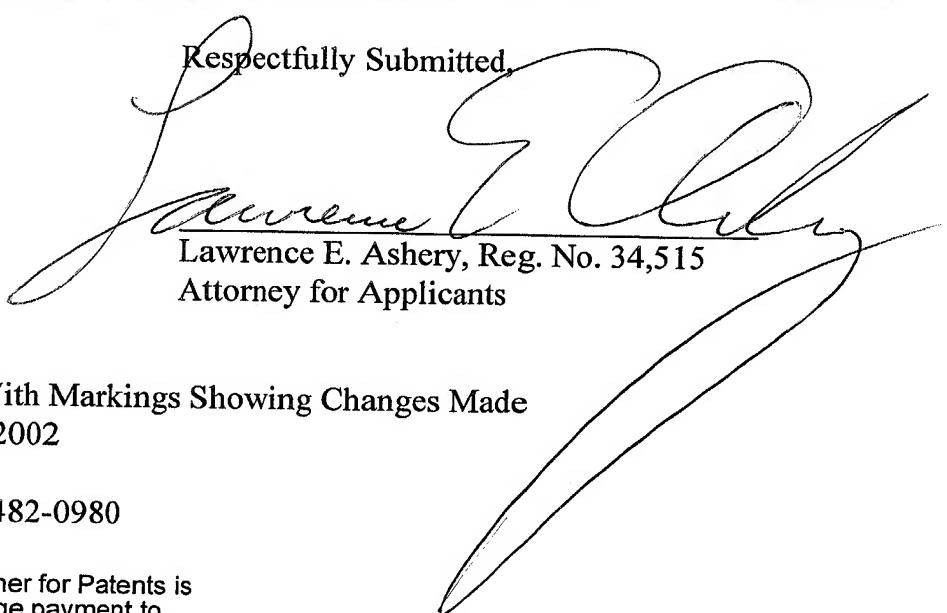
1        26. (Newly Added) The multilayer ceramic substrate of claim 14, further  
2 comprising an LSI chip mounted on a part of one of said first and second  
3 conductive patterns with the face down and electrically connected.

1        27. (Newly Added) The multilayer ceramic substrate of claim 14, further  
2 comprising an LSI chip mounted on a part of one of said first and second  
3 conductive patterns with the face down and electrically connected through an  
4 electroconductive paste applied on the top of a fine bump provided on one of said

5 first and second conductive patterns, said fine bump formed by using a second  
6 groove which is disposed on said intaglio at a place corresponding to a pad of said  
7 LSI chip.

1 28. (Newly Added) The multilayer ceramic substrate of claim 14, further  
2 comprising an LSI package mounted on a part of one of said first and second  
3 conductive patterns with the face down and electrically connected through a lattice  
4 of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said  
5 first and second conductive patterns.

Respectfully Submitted,

  
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Enclosure: Version With Markings Showing Changes Made

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Kathleen Libby

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